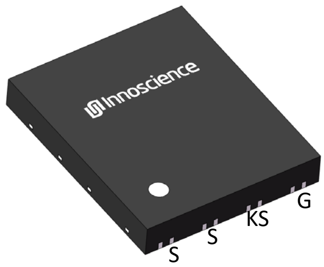
INN700DC240A

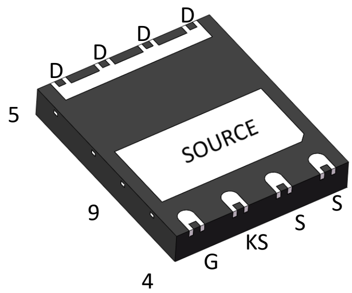
1. General description

700V GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 5 mm × 6 mm size

2. Features

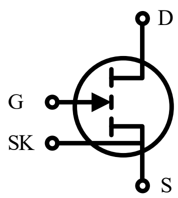


- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion



4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	240	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	2	nC
$I_{D,pulse}$	18	A
Q_{OSS} @ V_{DS} = 400 V	21	nC
Q_{rr} @ V_{DS} = 400 V	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
4	5, 6, 7, 8	3	1, 2, 9

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN700DC240A	DFN 5X6	70DC240A

Table of contents

1. General description 1
2. Features 1
3. Applications 1
4. Key performance parameters 1
5. Pin information 1
6. Maximum ratings 3
7. Thermal characteristics 4
8. Electric characteristics 5
9. Electric characteristics diagrams 7
10. Package outlines 13
11. Reel information 14
12. Recommended PCB footprint 15
13. Revision history 16

6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,\ max}$	700	V	V_{GS} = 0 V; T_j = -55 °C to 150 °C
Drain source voltage transient [1]	$V_{DS,\ transient}$	800	V	V_{GS} = 0 V
Drain source voltage, pulsed [2]	$V_{DS,\ pulse}$	750	V	T_j = 25 °C; total time < 10 h
				T_j = 125 °C; total time < 1 h
Continuous current, drain source	I_D	10	A	T_c = 25 °C
Pulsed current, drain source [3]	$I_{D,\ pulse}$	18	A	T_c = 25 °C; V_{GS} = 6 V; t_{PULSE} = 300 μs
Pulsed current, drain source [3]	$I_{D,\ pulse}$	10	A	T_c = 125 °C; V_{GS} = 6 V; t_{PULSE} = 300 μs
Gate source voltage, continuous [4]	V_{GS}	-1.4 to +7	V	T_j = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS,\ pulse}$	-20 to +10	V	T_j = -55 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	75	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	˚C	
Storage temperature	T_{stg}	-55 to +150	˚C	

1. $V_{DS,\ transient}$ is intended for non-repetitive events, t_{PULSE} < 200 μs.
2. $V_{DS,\ pulse}$ is intended for repetitive pulse, t_{PULSE} < 100 ns.
3. Limit was extracted from characterization test, not measured during production.
4. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10.

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA}	60.8	°C/W	
Thermal resistance, junction-case	R_{thJC}	1.65	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	MSL3

8. Electric characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	I_D = 11 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.7	-		I_D = 11 mA; V_{DS} = V_{GS}; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	0.4	20	μA	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C
		-	5	-		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	50	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	165	240	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 25 °C
		-	360	-	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 150 °C
Gate resistance	R_G	-	5	-	Ω	f = 5 MHz; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	79	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	25	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.2	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	36	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	52	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	21	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	2	-	ns	V_{DS} = 400 V; I_D = 6 A; L = 318 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω; See Figure 22
Turn-off delay time	$t_{d(off)}$	-	4	-	ns	
Rise time	t_r	-	5	-	ns	
Fall time	t_f	-	6	-	ns	

1. $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.

2. $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 8 Gate charge characteristics

Parameter	Symbol	Values Min.	Values Typ.	Values Max.	Unit	Note/Test Condition
Gate charge	Q_G	-	2	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 3 A
Gate-source charge	Q_{GS}	-	0.2	-	nC	
Gate-drain charge	Q_{GD}	-	0.7	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.5	-	V	V_{DS} = 400 V; I_D = 3 A

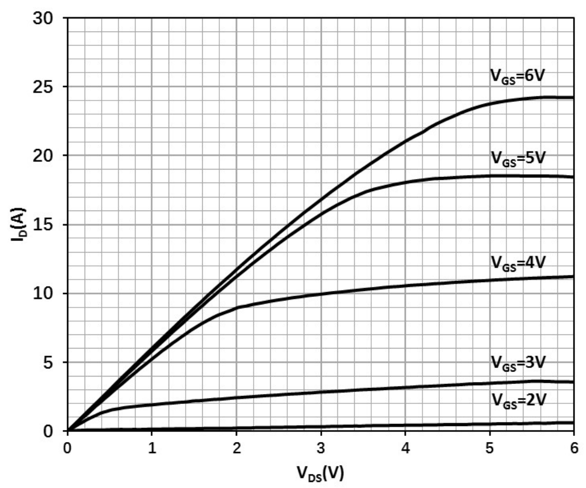
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values Min.	Values Typ.	Values Max.	Unit	Note/Test Condition
Source-Drain reverse voltage	V_{SD}	-	2.6	-	V	V_{GS} = 0 V; I_S = 3 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	-	18	A	V_{GS} = 6 V; t_{PULSE} = 300 µs
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_S = 3 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

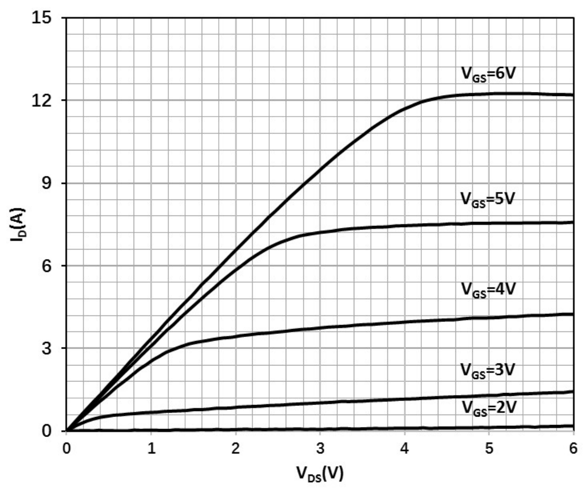
at T_j = 25 °C, unless specified otherwise

Figure 1 Typ. output characteristics



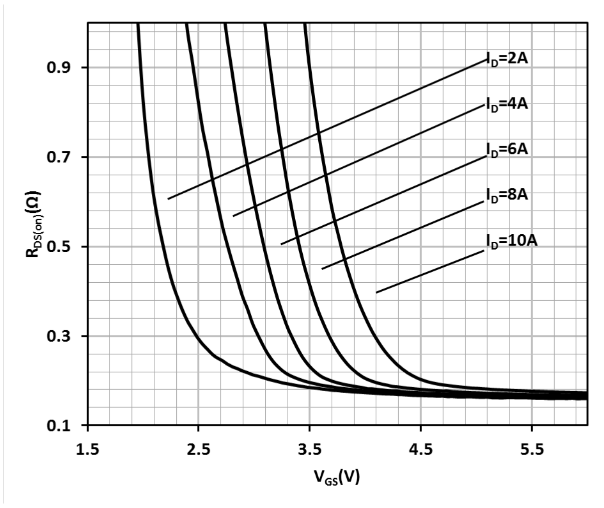
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



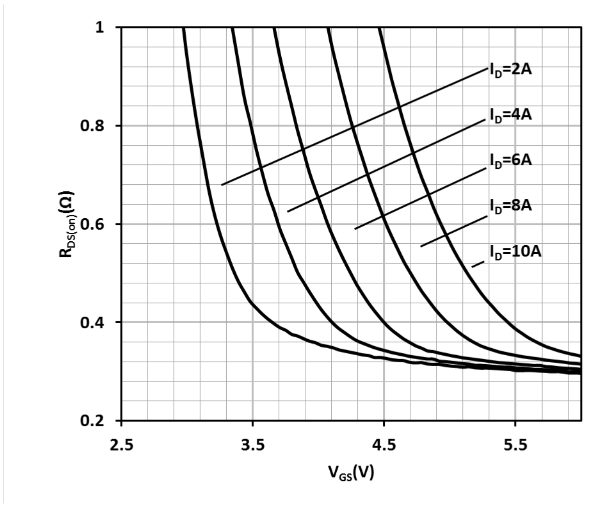
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 3 Typ. Drain-source on-state resistance



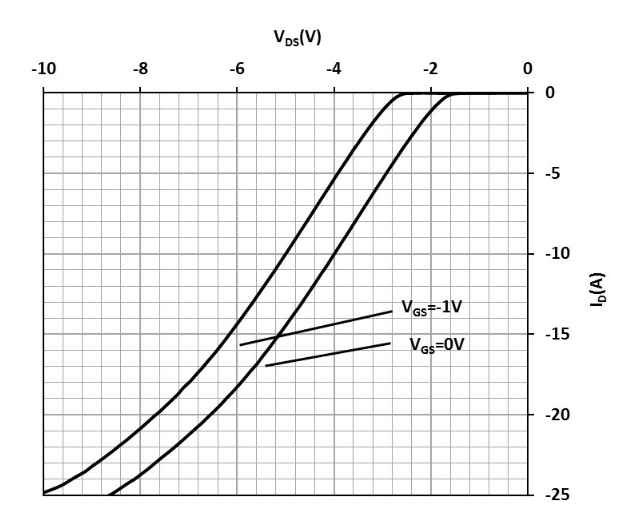
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 25 °C

Figure 4 Typ. Drain-source on-state resistance



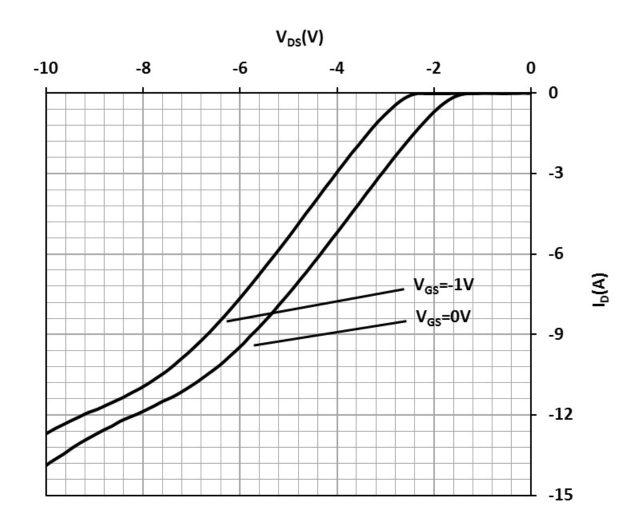
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



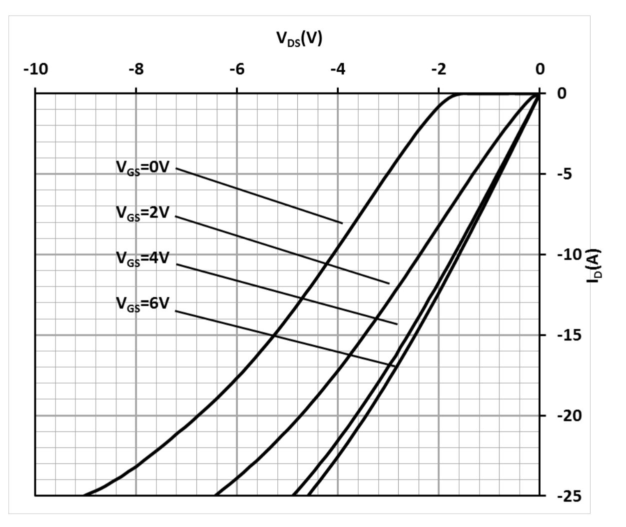
$I_D = f(V_{DS}, V_{GS})$; T_j= 25 °C

Figure 6 Typ. channel reverse characteristics



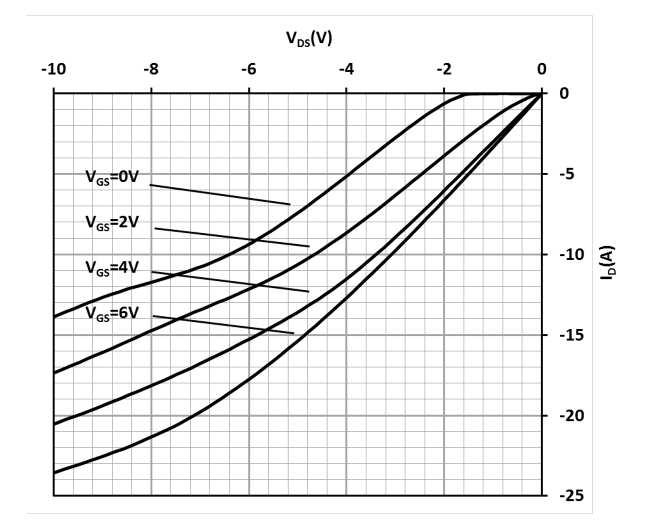
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 7 Typ. channel reverse characteristics



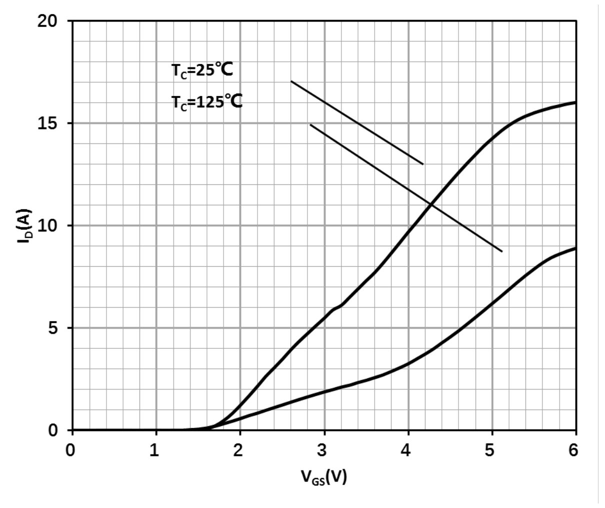
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 8 Typ. channel reverse characteristics



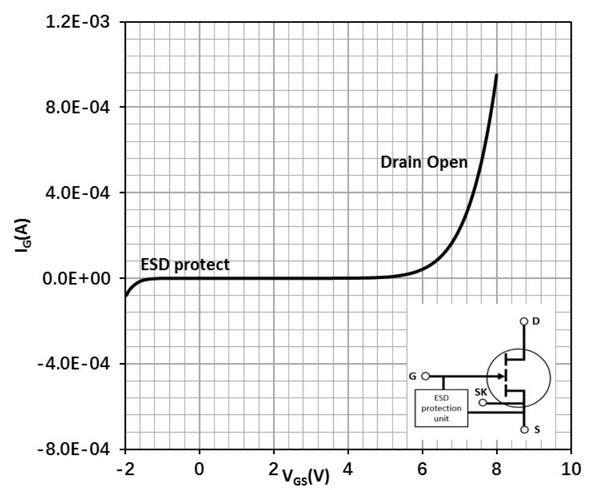
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 9 Typ. transfer characteristics



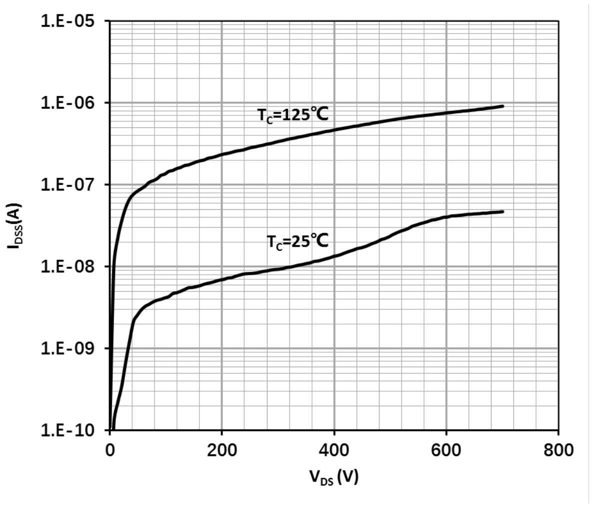
$I_D = f(V_{GS})$; V_{DS}= 3 V

Figure 10 Typ. Gate-to-Source leakage



$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

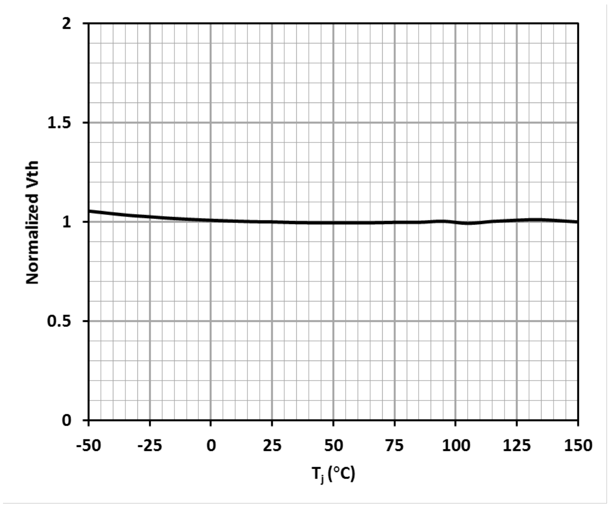
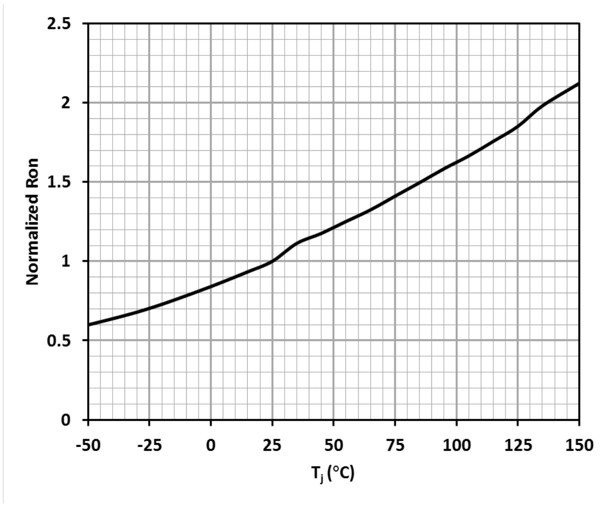
Figure 12 Gate threshold voltage	Figure 13 Drain-source on-state resistance
	
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 11 mA	$R_{DS(on)} = f(T_j)$; I_D = 3 A; V_{GS}=6V

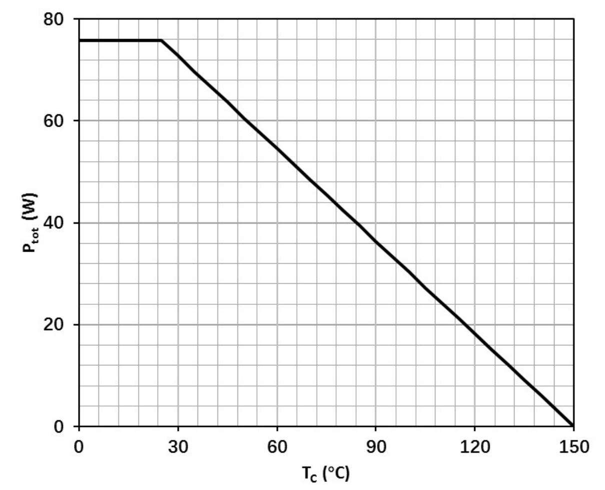
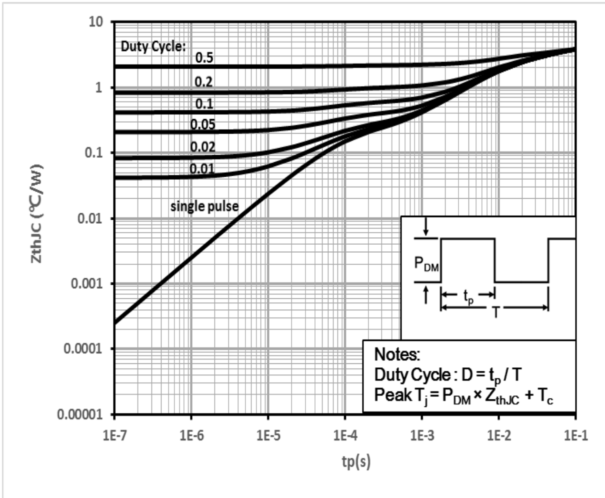
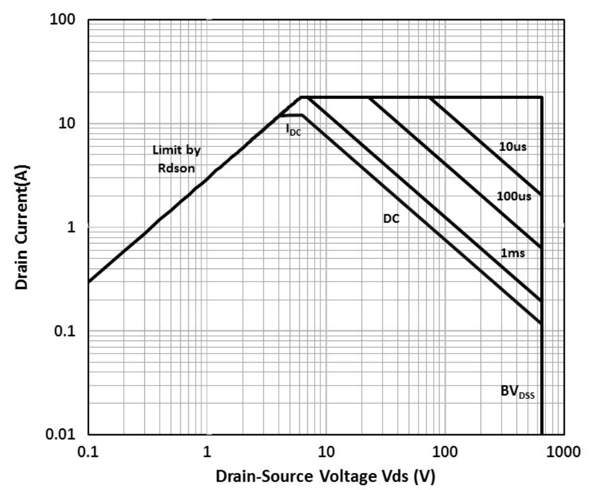
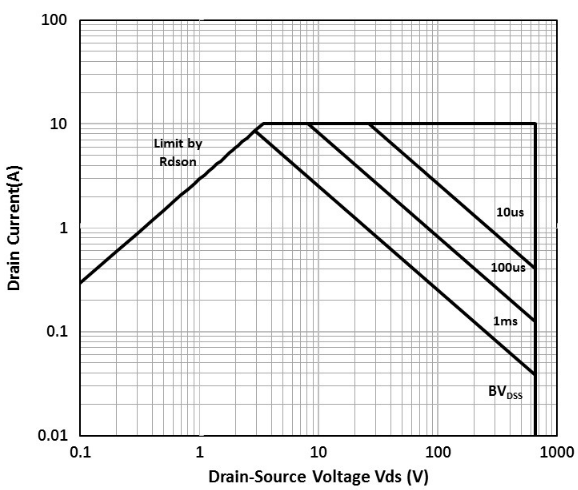
Figure 14 Power dissipation	Figure 15 Max.transient thermal impedance
	
$P_{tot} = f(T_C)$	$Z_{thJC} = f(t_P, D)$

Figure 16 Safe operating area



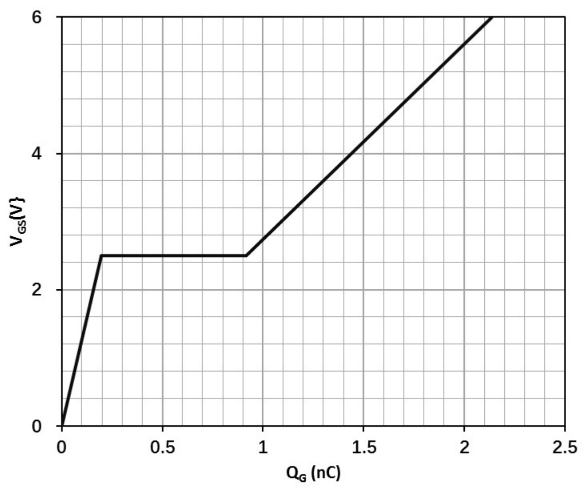
$I_D = f(V_{DS})$; T_C = 25 °C

Figure 17 Safe operating area



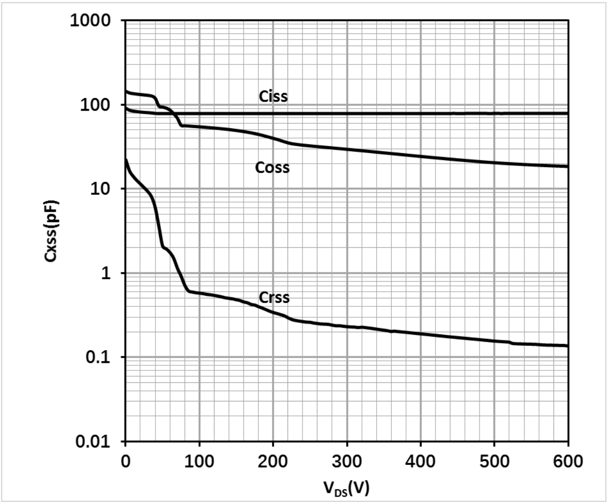
$I_D = f(V_{DS})$; T_C = 125 °C

Figure 18 Typ. gate charge



$V_{GS} = f(Q_G)$; V_{DCLINK} = 400 V; I_D = 3 A

Figure 19 Typ. capacitances



$C_{XSS} = f(V_{DS})$; Freq. = 100 kHz

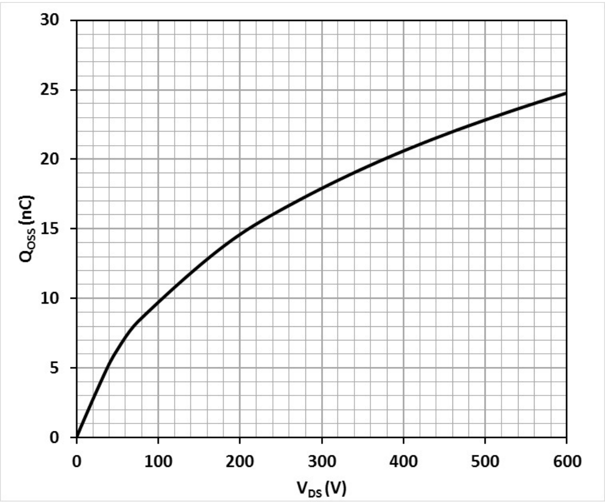
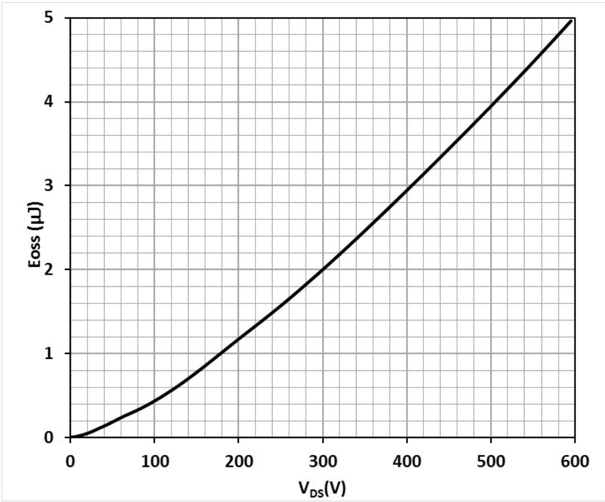
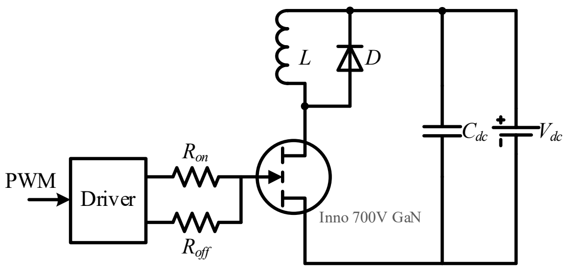
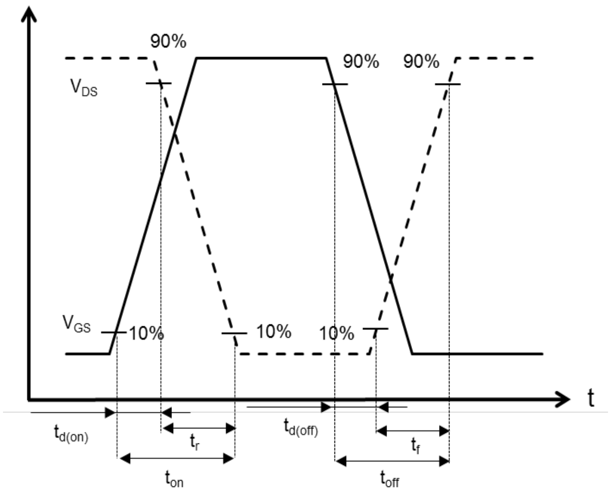
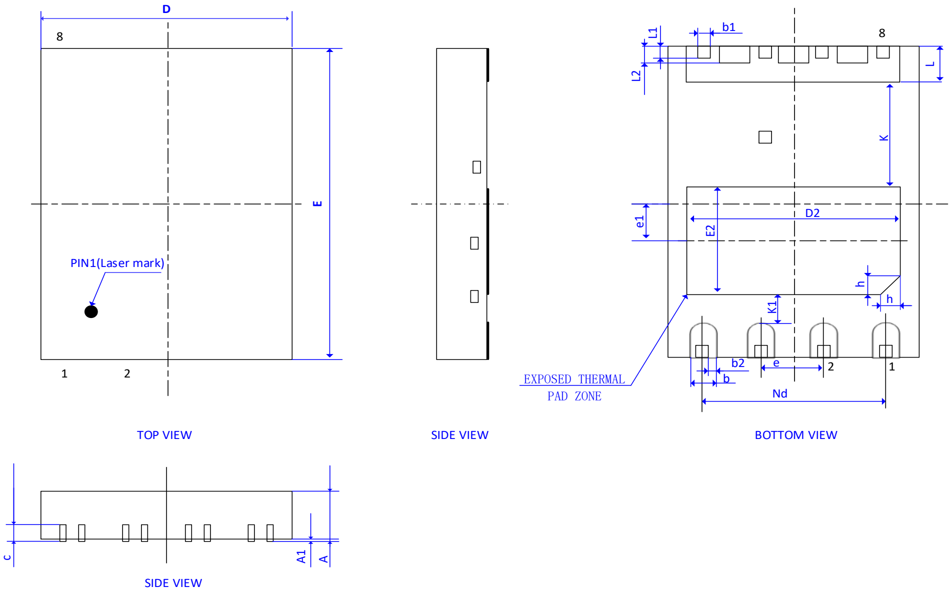
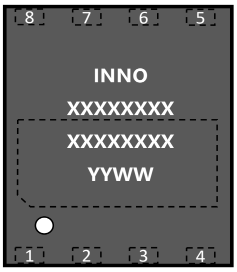
Figure 20 Typ. output charge	Figure 21 Typ. C_{OSS} stored Energy
	
$Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz	$E_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 22 Typ.Switching times with inductive load	Figure 23 Typ.Switching times waveform
	
V_{DS} = 400 V, I_D = 6 A, L = 318 µH, V_{GS} = 6 V, R_{on} = 10 Ω, R_{off} = 2 Ω	

10. Package outlines



SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.80	0.85	0.90	Nd	3.81BSC		
A1	0.00	0.02	0.05	E	5.90	6.00	6.10
b	0.40	0.45	0.50	E2	1.95	2.05	2.15
b1	0.20REF			L	0.625	0.675	0.725
b2	0.125REF			L1	0.15REF		
c	0.203REF			L2	0.25REF		
D	4.90	5.00	5.10	h	0.30	0.35	0.40
D2	4.16	4.26	4.36	K	2.1REF		
e	1.27BSC			K1	0.50REF		
e1	0.80BSC						

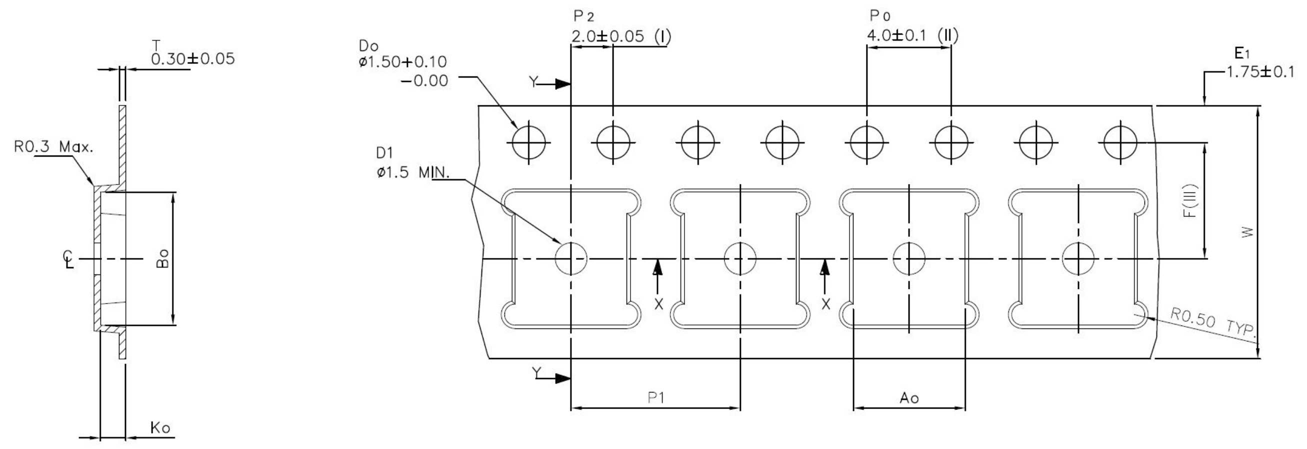


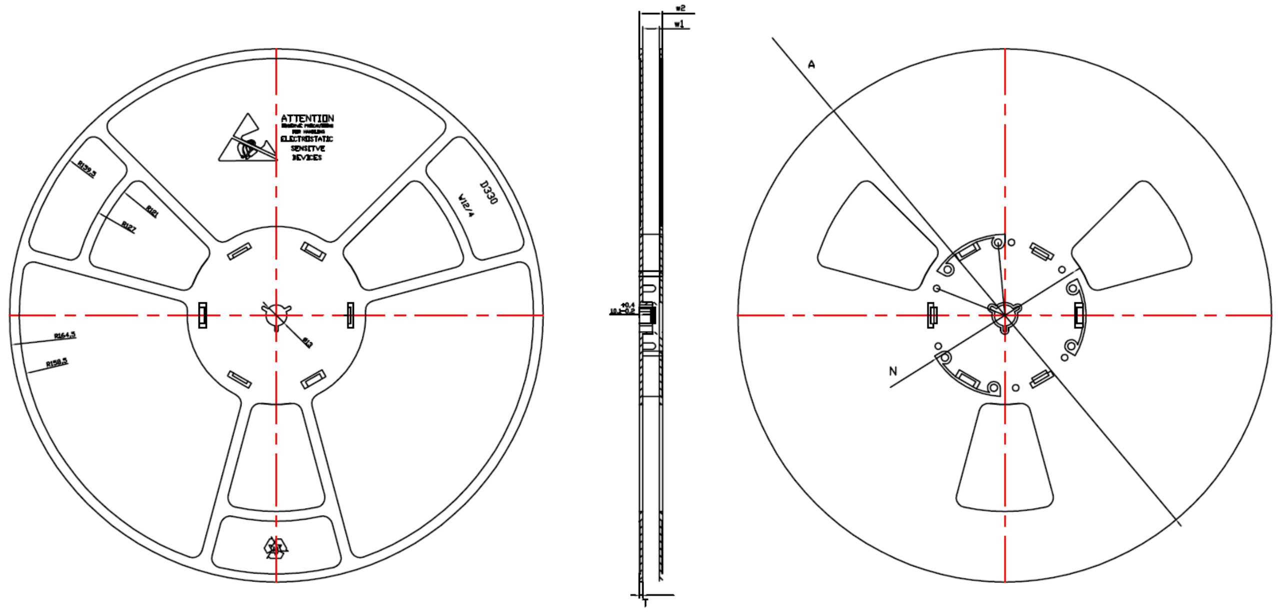
Row	Description	Example
Row1	Company name	INNO
Row2	Product code (In short)	XXXXXXXX
Row3	ASSY lot No.	XXXXXXXX
Row4	Date code	YYWW

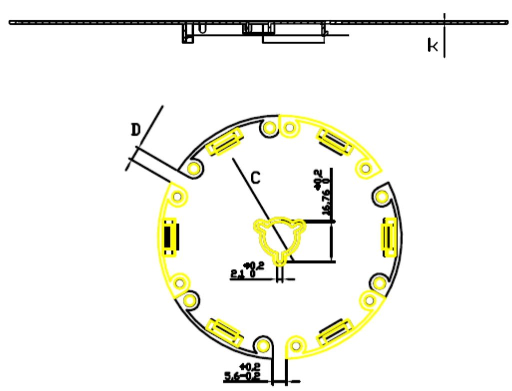
Notes:

(1) Dimension and tolerance conform to ASME Y14.5-2009.
(2) All dimension are in millimeters.
(3) Lead coplanarity shall be 0.1 millimeters max.
(4) Complies with JEDEC MO-229.
(5) Drawing is not to scale.
(6) Dimensions do not include mold protrusion.
(7) Package outline exclusive of metal burr dimensions.

11. Reel information

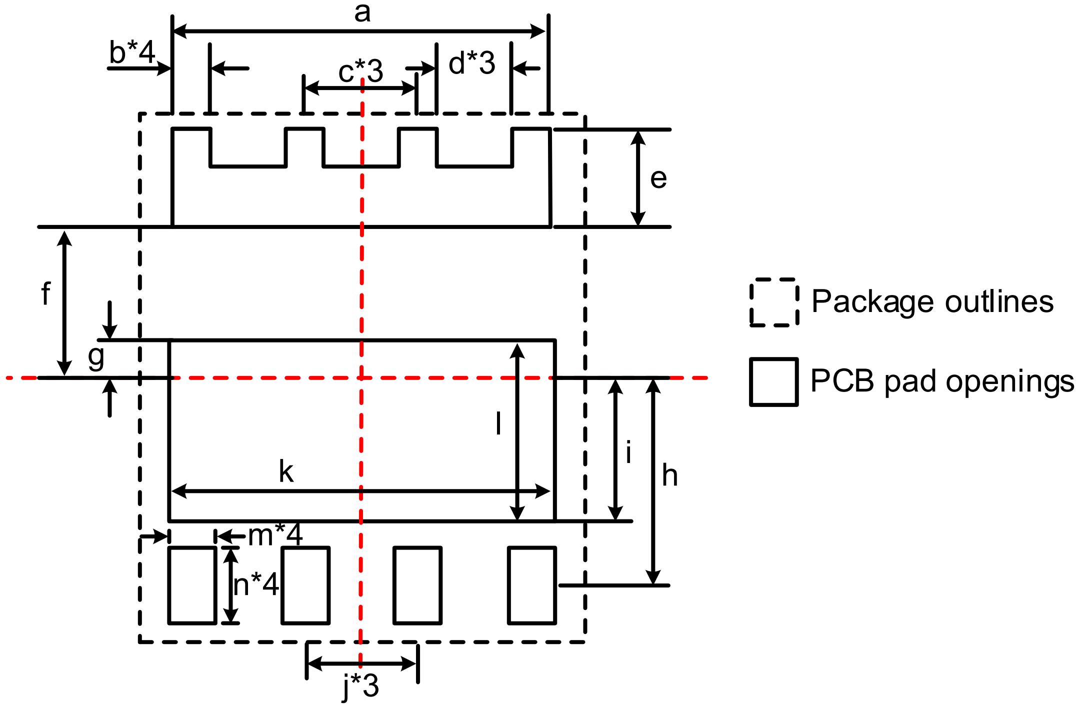






SYMBOL	DIMENSION(mm)		
	MIN	NOM	MAX
A_0	5.20	5.30	5.40
B_0	6.20	6.30	6.40
K_0	1.10	1.20	1.30
F	5.45	5.50	5.55
P1	7.90	8.00	8.10
W	11.70	12.00	12.30
A	328	330	332
N	98	100	102
C	12.90	13.10	13.30
D	5.10	5.60	6.10
w1	12.40	12.40	14.40
w2	16.60	16.60	18.60
T	1.95	2.10	2.25
K	1.30	1.40	1.55

12. Recommended PCB footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	4.340	h	2.900
b	0.530	i	1.875
c	1.270	j	1.270
d	0.740	k	4.360
e	1.190	l	2.150
f	2.315	m	0.550
g	0.275	n	1.000

Notes:
(1) All dimension are in millimeters.
(2) Drawing is not to scale.

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-08-20	1.0 version release

Important Notice